What is Claimed is:

1. A programmable logic device comprising:

a programmable logic device configuration control block;

a plurality of programmable logic device core building blocks that are programmable based on signals received from the configuration control block;

a management data input/output configuration control block that receives signals from the core building blocks; and

a plurality of embedded intellectual property building blocks that are configurable based on signals received from the management data input/output configuration control block or signals received from the programmable logic device configuration control block.

2. The programmable logic device of claim 1 wherein the management data input/output configuration control block is adapted to receive status information relating to the protocol of the programmable embedded intellectual property building blocks.

3. The programmable logic device of claim 1 wherein the management data input/output configuration control block is adapted to exchange status information relating to the protocol of the embedded intellectual property building blocks with the PLD core building blocks.

4. The programmable logic device of claim 1 further comprising a selection logic block that is adapted to select between signals received from the

management data input/output configuration control block and signals received from the programmable logic device configuration control block and to transmit the selected signals for configuring the programmable embedded IP building blocks.

5. The programmable logic device of claim 4 wherein the selection logic block selects based on signals received from the programmable logic device core building blocks.

6. The programmable logic device of claim 1 wherein the management data input/output configuration control block configures the programmable embedded intellectual property building blocks using a plurality of frames.

7. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 1 coupled to the processing circuitry and the memory.

8. A printed circuit board on which is mounted a programmable logic device as defined in claim 7.

9. The printed circuit board defined in claim 8 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

10. The printed circuit board defined in claim 9 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

11. A method for changing the protocol supported by embedded intellectual property building blocks in a programmable logic device, the method comprising:

configuring the protocol of the embedded intellectual property building blocks during configuration of the programmable logic device;

commencing operation of the programmable logic device; and

during operation of the programmable logic device, dynamically reconfiguring the protocol of the programmable logic device.

12. The method of claim 11 further comprising transmitting status information relating to the embedded intellectual property building blocks to a plurality of programmable logic device core building blocks.

13. The method of claim 12 wherein the transmitting further comprises transmitting via a management data input/output configuration control block.

14. The method of claim 11 further comprising transmitting status information relating to

the protocol supported by the embedded intellectual property building blocks to a plurality of programmable logic device core building blocks.

15. The method of claim 11 further comprising using signals provided by a management data input/output configuration control block to reconfigure the embedded IP building blocks.

16. The method of claim 11 further comprising using signals provided by a programmable logic device configuration control block to configure the embedded IP building blocks.

17. The method of claim 11 further comprising selecting between signals provided by a management data input/output configuration control block and signals provided by a programmable logic device configuration control block, the selected signals for configuring the embedded IP building blocks.

18. The method of claim 11 wherein the signals provided by the management data input/output configuration control block are provided using a plurality of frames.